REMARKS

Claims 1-49 are pending. Claims 1, 17, 26, 33, 36, 42, and 46 are in independent form.

CLAIM 1

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,741,258 to Peck, Jr. et al. (hereinafter "Peck") and U.S. Patent No. 6,085,296 to Karkhanis et al. (hereinafter "Karkhanis").

Claim 1 relates to a machine-implemented method that includes receiving, by a first process in a first user virtual memory address space, a shortcut to a physical address associated with a level of a multi-level virtual address translation table, posting a descriptor to an interface between the first process and a second process, and determining, by the second process, the physical address corresponding to the virtual address based on at least the virtual address and the shortcut. The descriptor includes a virtual address in the first user virtual memory address space and the shortcut. The second process is in a second user virtual memory address space.

The rejection of claim 1 is based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, Peck describes a system in which a multiple processing devices can access a single main memory device. See, e.g., Peck, FIG. 1; col. 4, line 38-41. A collection of interface units 22a, 22b, 22c, and 22d each support an interface between the main memory device and a specific processing device. *See, e.g., id.*, col. 4, line 33-37. Each interface unit includes a separate translation look-aside buffer. *See, e.g., id.*, col. 4, line 50-51.

Each interface unit operates independently to support the translation of linear addresses for its corresponding processing device. *See, e.g., id.*, col. 5, line 45-48. Indeed, Peck describes that such independent address translation for different processing devices is favorable. *See, e.g., id.*, col. 6, line 6-32 (describing that separate translation look-aside buffers eliminate contention for use of the same buffer storage space, make the processes of address translation and data retrieval more efficient, reduce the duration of interconnections, and enhance overall system operation).

However, nothing in Peck involves address translation for different processes and/or processing devices.

Against this backdrop, the rejection of claim 1 contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a descriptor that includes a virtual address in a first user virtual memory address space and a shortcut to a physical address is posted to an interface between the first process and a second process, as recited in claim 1. The rejection of claim 1 also contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that the physical address corresponding to the virtual address is determined by the second process based on at least the virtual address and the shortcut, as recited in claim 1.

Applicant respectfully disagrees. In this regard, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables. *See, e.g., Karkhanis*, col. 4, line 56-58. Karkhanis' processes are thus in the same user virtual memory address space.

Since Karkhanis' processes all share the same virtual memory address translation page tables and are in the same user virtual memory address space, Karkhanis neither describes nor suggests that a descriptor that includes a virtual address in a first user virtual memory address space and a shortcut to a physical address is posted to an interface between the first process and a second process, as recited in claim 1. Moreover,

neither describes nor suggests that the physical address corresponding to the virtual address is determined by a second process based on at least the virtual address and the shortcut, as recited in claim 1. Instead, Karkhanis' processes simply use the shared virtual memory address translation page tables.

Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claim 1. Accordingly, claim 1 is not obvious over Peck and Karkhanis. Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 17

Claim 17 was rejected under 35 U.S.C. § 103(a) as obvious over Peck and Karkhanis.

Claim 17 relates to a machine-implemented method. The method includes generating, by a first user process in a first user virtual memory address space, a request to register a virtual buffer, identifying a block of memory that includes the physical address corresponding to the start of the virtual buffer, generating, by a second process, one or more shortcuts that map the block of memory that includes the physical address corresponding to the start of the virtual buffer, and transmitting a request to a third user process in a second user virtual memory address space to perform an input or output

operation on the virtual buffer. The virtual buffer is in the first user virtual memory address space and is mapped to physical memory by a multi-level virtual address translation table associated with the first process.

The rejection of claim 17 is based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, as discussed above, Peck describes a system in which multiple interface units operate independently to support the translation of linear addresses for a corresponding processing device. However, nothing in Peck involves address translation for different processes and/or processing devices. Instead, Peck describes that independent address translation for different processing devices is favorable.

Against this backdrop, the rejection of claim 17 contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a request is transmitted to a third user process in a second user virtual memory address space to perform an input or output operation on a virtual buffer that is in a first user virtual memory address space, as recited in claim 17.

Applicant respectfully disagrees. In this regard, as discussed above, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables. Karkhanis' processes are thus in the same user virtual memory address space.

Since Karkhanis' processes are all in the same user virtual memory address space, Karkhanis neither describes nor suggests that a request is transmitted to a third user process in a second user virtual memory address space to perform an input or output operation on a virtual buffer that is in a first user virtual memory address space, as recited in claim 17. Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claim 17.

Accordingly, claim 17 is not obvious over Peck and Karkhanis. Applicant requests that the rejections of claim 17 and the claims dependent therefrom be withdrawn.

CLAIM 26

Claim 26 was rejected under 35 U.S.C. § 103(a) as obvious over Peck and Karkhanis.

Claim 26 relates to a system that includes a first processor and a second processor. The first processor is configured to execute instructions of a first process which causes the first processor to produce a shortcut to a physical

address associated with a level of a multi-level virtual address translation table, and execute instructions of a second user process in a first user virtual memory address space which causes the first processor to post a descriptor comprising a virtual address and the shortcut to an interface. The second processor is configured to execute instructions of a third user process in a second user virtual memory address space which cause the second processor to read the descriptor posted on the interface, and determine a physical address of the virtual address based on at least the virtual address and the shortcut. The interface is between the second process and the third process.

The rejection of claim 26 is based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, as discussed above, Peck describes a system in which multiple interface units operate independently to support the translation of linear addresses for a corresponding processing device. However, nothing in Peck involves address translation for different processes and/or processing devices. Instead, Peck describes that independent address translation for different processing devices is favorable.

Against this backdrop, the rejection of claim 26 contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a second processor configured to execute instructions of a user process in a second user virtual memory address space is to read a descriptor posted on the interface between the second process and the third process and determine a physical address of a virtual address based on at least the virtual address and the shortcut posted by first processor executing instructions of a second user process in a first user virtual memory address space, as recited in claim 26.

Applicant respectfully disagrees. In this regard, as discussed above, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables and are in the same user virtual memory address space.

Since Karkhanis' processes all share the same virtual memory address translation page tables and are in the same user virtual memory address space, Karkhanis neither describes nor suggests that a second processor configured to execute instructions of a user process in a second user virtual memory address space is to read a descriptor posted on the interface between the second process and the third process and determine a physical address of a virtual address based on at least the virtual address and the shortcut posted by first processor executing instructions of a second user process in a first user

virtual memory address space, as recited in claim 26. Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claim 26.

Accordingly, claim 26 is not obvious over Peck and Karkhanis. Applicant requests that the rejections of claim 26 and the claims dependent therefrom be withdrawn.

CLAIM 33

Claim 33 was rejected under 35 U.S.C. § 103(a) as obvious over Peck and Karkhanis.

Claim 33 relates to a computer program product residing on a computer readable medium having instructions stored thereon. When the instructions are executed by the processor, the instructions cause that processor to produce a shortcut to a physical address associated with a level of a multi-level virtual address translation table, and write a descriptor comprising a virtual address and the shortcut to an interface between a first user process in a first user virtual memory address space and a second user process in a second user virtual memory address space.

The rejection of claim 33 is based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, as discussed above, Peck describes a system in which multiple interface units operate independently to support the translation of linear addresses for a corresponding processing device. However, nothing in Peck involves address translation for different processes and/or processing devices. Instead, Peck describes that independent address translation for different processing devices is favorable.

Against this backdrop, the rejection of claim 33 contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a processor writes a descriptor comprising a virtual address and a shortcut to an interface between a first user process in a first user virtual memory address space and a second user process in a second user virtual memory address space, as recited in claim 33.

Applicant respectfully disagrees. In this regard, as discussed above, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables and are in the same user virtual memory address space.

Since Karkhanis' processes all share the same virtual memory address translation page tables and are in the same user virtual memory address space, Karkhanis neither describes nor suggests that that a processor writes a descriptor comprising a virtual address and a shortcut to an interface between a first

user process in a first user virtual memory address space and a second user process in a second user virtual memory address space, as recited in claim 33. Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claim 33.

Accordingly, claim 33 is not obvious over Peck and Karkhanis. Applicant requests that the rejections of claim 33 and the claims dependent therefrom be withdrawn.

CLAIM 36

Claim 36 was rejected under 35 U.S.C. § 103(a) as obvious over Peck and Karkhanis.

Claim 36 relates to a computer program product residing on a computer readable medium having instructions stored thereon. When the instructions are executed by a processor performing operations in a first user virtual memory address space, they cause that processor to read a message posted on an interface by a first user process in a different user virtual memory address space, the message including a shortcut to a physical address associated with a level of a multi-level virtual address translation table, determine a physical address of a virtual address in the different user virtual memory address space based

on at least the virtual address and the shortcut, and transmit a message over a network based on contents of the physical address.

The rejection of claim 36 is based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, as discussed above, Peck describes a system in which multiple interface units operate independently to support the translation of linear addresses for a corresponding processing device. However, nothing in Peck involves address translation for different processes and/or processing devices. Instead, Peck describes that independent address translation for different processing devices is favorable.

Against this backdrop, the rejection of claim 36 contends that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a processor performing operations in a first user virtual memory address space reads a message posted on an interface by a first user process in a different user virtual memory address space and determines a physical address of a virtual address in the different user

virtual memory address space based on at least a virtual address and the shortcut included in the read message, as recited in claim 36.

Applicant respectfully disagrees. In this regard, as discussed above, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables and are in the same user virtual memory address space.

Since Karkhanis' processes all share the same virtual memory address translation page tables and are in the same user virtual memory address space, Karkhanis neither describes nor suggests that that a processor performing operations in a first user virtual memory address space reads a message posted on an interface by a first user process in a different user virtual memory address space and determines a physical address of a virtual address in the different user virtual memory address space based on at least a virtual address and the shortcut included in the read message, as recited in claim 36.

Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claim 36.

Accordingly, claim 36 is not obvious over Peck and Karkhanis. Applicant requests that the rejections of claim 36 and the claims dependent therefrom be withdrawn.

CLAIMS 42 AND 46

Claims 42 and 46 were rejected under 35 U.S.C. § 103(a) as obvious over Peck and Karkhanis.

Claim 42 relates to a system that includes a client computer and a server in communication with the client computer using a network. The server includes a first processor and a second processor. The first processor is configured to produce a shortcut to a physical address associated with a level of a multi-level virtual address translation table and write a descriptor comprising a virtual address in a first user virtual memory address space and the shortcut to an interface. The second processor is configured to perform operations in a second user virtual memory address space, the operations including reading the descriptor posted on the interface, determining a physical address of the virtual address based on at least the virtual address and the shortcut, and transferring data located at the physical address to the client computer using the network.

As amended, claim 46 relates to a system that includes a storage device and a server in communication with the storage device over a network. The server of claim 46 is otherwise comparable to the server of claim 42.

The rejections of claim 42 and 46 are based on the contention that it would have been obvious for one of ordinary skill to have combined Peck and Karkhanis and arrive at the recited subject matter.

Applicant respectfully disagrees. In this regard, as discussed above, Peck describes a system in which multiple interface units operate independently to support the translation of linear addresses for a corresponding processing device. However, nothing in Peck involves address translation for different processes and/or processing devices. Instead, Peck describes that independent address translation for different processing devices is favorable.

Against this backdrop, the rejections of claims 42 and 46 contend that it would be obvious for one of ordinary skill to modify Peck based on Karkhanis so that a first processor writes a descriptor comprising a virtual address in a first user virtual memory address space and a shortcut to an interface and a second processor, which is configured to perform operations in a second user virtual memory address space, reads the descriptor posted on the interface and determines a physical address of the virtual address based on at least the virtual address and the shortcut, as recited in claims 42 and 46.

Applicant respectfully disagrees. In this regard, as discussed above, Karkhanis describes a system in multiple processes all share virtual memory address translation page tables and are in the same user virtual memory address space.

Since Karkhanis' processes all share the same virtual memory address translation page tables and are in the same user virtual memory address space, Karkhanis neither describes nor suggests that that a first processor writes a descriptor comprising a virtual address in a first user virtual memory address space and a shortcut to an interface and a second processor, which is configured to perform operations in a second user virtual memory address space, reads the descriptor posted on the interface and determines a physical address of the virtual address based on at least the virtual address and the shortcut, as recited in claims 42 and 46.

Thus, even if Peck and Karkhanis were combined (which applicant does not concede), one of ordinary skill would still not arrive at the subject matter recited in claims 42 and 46.

Accordingly, claims 42 and 46 are not obvious over Peck and Karkhanis. Applicant requests that the rejections of claims 42 and 46 and the claims dependent therefrom be withdrawn.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. Please apply the one-month extension of time fee and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: August 20, 2007

Scott C. Harris
Reg. No. 32,030

BY
JOHN F. CONROY
REG. NO. 45,485

Fish & Richardson P.C.
PTO Customer No. 20985
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

SCH/JFC/jhg
10765285.doc